Flash A-D Converter

Also called the *parallel A/D converter*, this circuit is the simplest to understand. It is a series of comparators, each one comparing the input signal to a unique reference voltage. The comparator outputs connected to the inputs of a priority encoder circuit, which then produces a binary output.

They are the fastest and simplest A/D converter. In an N-bit converter, 2^N-1 analog latching comparators and voltage references are used to convert the analog voltage to a digital word. N is the number of output bits.

Shows the diagram with the voltage divider resistor bridge and the comparators hooked to the output of the voltage divider, then going into the priority encoder. If the voltage input is 3.2516 volts, the lowest 5 comparators will be turned on and the others turned off.

A B-bit Flash A/D converter requires $2^B - 1$ comparators. Thus, an 8-bit flash A/D requires 255 comparators. 4095 for 12 bit; could not put that many on an IC at the time the slide was prepared. Largest flash comparator is 8 bits (at time slide was made).

Flash A/D converters can sample at several billion samples/second. Parallel gives this the speed advantage since there is no multiplier unlike with serial.

Reference Voltage

Vref is a stable reference voltage. It's provided by a precision voltage regulator and is part of the converter circuit. As the analog voltage input exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state. The priority encoder generates a binary number based on the highest-order active input, ignoring all other active inputs.

Flash Converter

Simplest in terms of operational theory. Most efficient of the ADC technologies in terms of speed, being limited only in comparator and gate propagation delays.

Most component intensive. In video we use 10 bits, so we'd have to have 1023 comparators.

Resistors need to be precision.

Ability to produce a nonlinear output. With equal value resistors in the reference voltage divider network, each successive binary count represents the same amount of analog signal increase, providing a proportional response. The resistor values in the divider network may be made non-equal. This gives the ADC a custom, nonlinear response to the analog input signal. Not other ADC design can modify signal-conditioning behavior with just a few component value changes. What would be want to be nonlinear? Could implement a knee that way, or gamma correction.

Half-flash

Two step ADC aka *subranging converters* and sometimes as *multi-step* or *half flash*. Cross between flash ADC and pipeline ADC and can achieve higher resolution and power for a given resolution are

needed vs. a flash ADC.

Diagram 1. Input voltage digitized by a coarse ADC filling bits 4-7. The output is converted back to an analog value. The converted value is subtracted from the original voltage forming an analog remainder. The remainder is digitized by a fine ADC filling bits 0-3. An external clock controls the latch insuring all steps are completed before the output is updated.

This results in two flash converters, but it saves a huge number of comparators. 30 comparators compared to 255 comparators.

This thing actually does an integer division by 16 to get the most significant nibble, then uses the result of the integer division to subtract from the original voltage, doing a modulo 16 operation on it to get the remainder of the integer division performed earlier to get the least significant nibble.

Pipeline (later)