Homework

Diagram 1

SMPTE time code Manchester encoding. Zero defined as no transition within a clock frame. One is defined as a transition within a clock frame.

Put data in, come out with a clock that is synchronous with our data.

Clock can be any multiple of the base frequency.

If sample ¼ of the way into the cycle, and ¾ of the way into the cycle, if there are different values at the two sample times, there is a 1 encoded, otherwise there are no differences between the two sample times and there is a 0 encoded.

The output data will actually be delayed/shifted by one clock cycle since we have to read the voltages during most of the cycle before we can decode the value.

Recall that a number of the complex chips we use are leading-edge-triggered, so would need to multiply the clock by 4 in order to get 4 edges within each 2400 Hz cycle so one can sample at ¼ and ¾ cycle.

Will grade papers today. If don't get it right, will have a chance to turn it in Thursday for a bit less credit.

Lab

Mostly spent time in lab today.